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10EE764

Seventh Semester B.E. Degree Examination, June/July 2017
VLSI Circuits and Design

Time: 3 hrs.

Max. Marks: 100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. Explain working of enhancement mode nMOS transistor for different values of V_{DS} with relevant diagrams. (06 Marks)
- b. Explain briefly nMOS fabrication process with neat sketches. (08 Marks)
- c. Compare CMOS and bipolar technologies. (06 Marks)
- 2 a. Derive expression for I_{ds} in non-saturated region of MOS devices. (06 Marks)
- b. Determine pull up to pull down ratio of an nMOS inverter driven directly by another nMOS inverter. (08 Marks)
- c. Explain Latch-up effect in p-well structure. (06 Marks)
- 3 a. Draw the stick diagram for a simple n-well based BiCMOS inverter. (06 Marks)
- b. Explain Lambda based design rules for MOS layers and transistors. (08 Marks)
- c. Explain nMOS design style with an example of stick layout for nMOS shift register cell. (06 Marks)
- 4 a. Calculate the resistance between V_{DD} and V_{SS} of nMOS inverter with pull up to pull down ratio = 4 and show that the ratio does not apply for CMOS inverter (Assume Lambda = 5 micro meters). (08 Marks)
- b. Explain concepts of sheet Resistance, standard unit of capacitance and Delay unit. (06 Marks)
- c. What are the advantages of super buffers? Explain non-inverting type nMOS super buffer with relevant diagram. (06 Marks)

PART – B

- 5 a. Explain briefly different scaling models with relevant diagram of nMOS transistor. (06 Marks)
- b. Obtain the scaling factors for the transistor parameters Gate capacitance, current. Density and power speed product in constant E and constant V scaling models. (08 Marks)
- c. Explain Electro-optical inter connection model with a neat diagram. (06 Marks)
- 6 a. Explain properties of pass transistors and transmission Gate. (06 Marks)
- b. Explain concept of Dynamic CMOS logic. (08 Marks)
- c. Explain structured design approach with an example of parity generator (nMOS). (06 Marks)
- 7 a. Explain some general considerations and problems associated with VLSI design. (06 Marks)
- b. With a neat diagram, explain design of 4 bit shifter. (08 Marks)
- c. Explain possible basic bus architectures for linking subunits of 4 bit digital processor. (06 Marks)
- 8 a. Explain 'Regularity' concept. (04 Marks)
- b. Explain multiplexer based adder logic (nMOS) with stored and buffered sum output. (08 Marks)
- c. Draw schematic of 4-bit ALU with Adder elements to perform logical operation and explain implementation. (08 Marks)

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